Features

- 48-pin TQFP
- Supports processor interface: byte/word of I/O command to internal memory data operation
- Integrated 10/100M transceiver with HP Auto-MDIX
- Supports back pressure mode for half-duplex mode flow control
- IEEE802.3x flow control for full-duplex mode
- Supports wakeup frame, link status change and magic packet events for remote wake up
- Support 100M Fiber interface.
- Integrated 16K Byte SRAM
- Build in 3.3V to 2.5V regulator
- Supports early Transmit
- Supports automatically load vendor ID and product ID from EEPROM
- Supports IP/TCP/UDP checksum generation and checking
- Optional EEPROM configuration
- Very low power consumption mode:

–Power reduced mode (cable detection)

–Power down mode

– Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction.

- Compatible with 3.3V and 5.0V tolerant I/O

Application

- Home network equipment: set top box, personal video recorder, digital media adapter
- Serial to Ethernet: access control, LED display, wireless AP relay, etc.
- Parallel to Ethernet: POS / micro printer, copier
- USB to Ethernet: storage device, network printer
- GPIO to Ethernet: home network sensor
- Security system: digital video recorder, network camera, information kiosk
- Factory and building automation control system
- Medical monitoring equipment
- Embedded Server

Catalog

Block Diagram

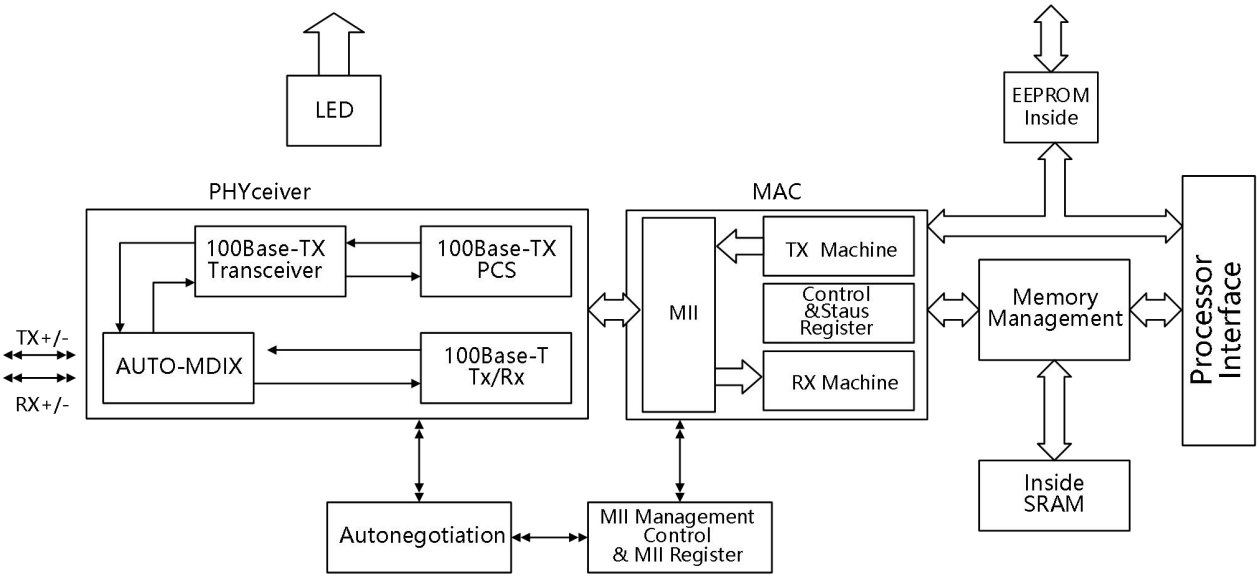

Figure 1. Block Diagram

Pin Configuration

16-bit mode

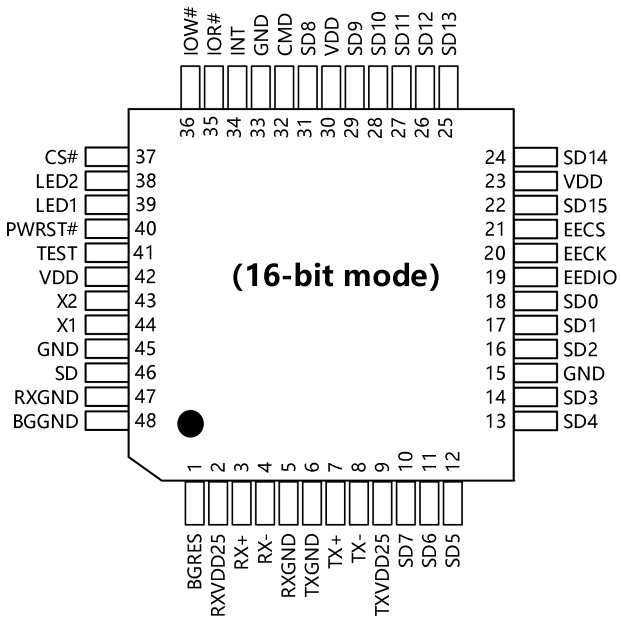

Figure 2. 16-bit mode Pin Assignment

8-bit mode

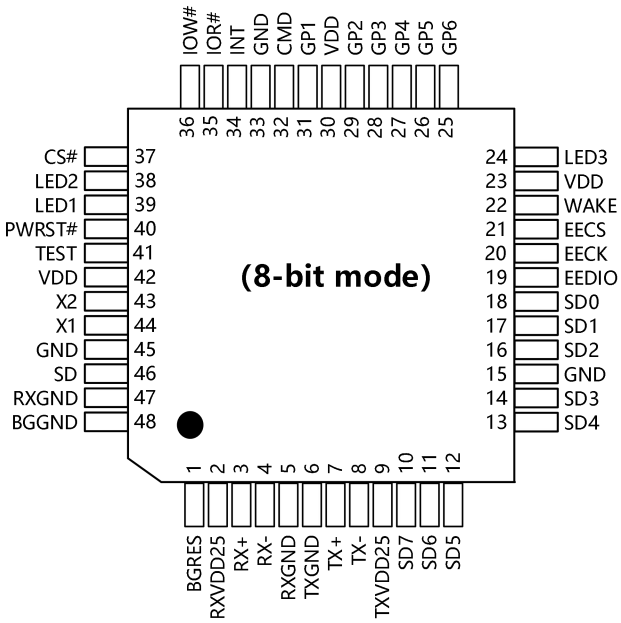

Figure 3. 8-bit mode

Pin Description

Pin No.	Pin Name	Type	Description
Processor Interface			
35	IOR#	I,PD	Processor Read Command
36	IOW#	I,PD	Processor Write Command
37	CS#	I,PD	Chip select
32	CMD	I,PD	Command Type
34	INT	O,PD	Interrupt Request
18,17,16,14,13,12,	SD0~7	I/O,PD	Processor Data Bus bit 0~7
11,10			
31,29,28,27,26,25,24,22	SD8~15	I/O,PD	Processor Data Bus bit 8~15
8-bit mode pins			
22	WAKE	O,PD	Issue a wake up signal when wake up event happens
24	LED3	O,PD	Full-duplex LED
25,26,27	GP6~4	O,PD	General Purpose output pins:
28,29,31	GP3,GP2,GP1	I/O	General I/O ports
EEPROM interface			
19	EEDIO	I/O,PD	IO data to eeprom
20	EECK	O,PD	Clock to eeprom
21	EECS	O,PD	Chip select to eeprom
Clock interface			
43	X2	O	Crystal 25Mhz out
44	X1	I	Crystal 25Mhz in
LED interface			
39	LED1	O	Speed LED
38	LED2	O	Link/Active LED
46	SD	I	Fiber-optic Signal Detect
48	BGGND	P	Bandgap Ground
1	BGRES	I/O	Bandgap Pin
2	RXVDD25	P	2.5V power output for TP RX

9	TXVDD25	P	2.5V power output for TP TX
3	RX+	I/O	TP RX Input
4	RX-	I/O	TP RX Input
5,47	RXGND	P	RX Ground
6	TXGND	P	TX Ground
7	TX+	I/O	TP TX output
8	TX-	I/O	TP TX output
Others			
41	TEST	I	Test mode
40	PWRST#	I	Power on reset
23,30,42	VDD	P	Digital VDD, 3.3V power input
15,33,45	GND	P	Digital GND

Register Description

MAC Register

Register	Description	Offset	Default value
NCR	Network register control	00H	00H
NSR	Network register status	01H	00H
NCR	TX register control	02H	00H
TSR I	TX register control I	03H	00H
TSR II	TX register control II	04H	00H
RCR	RX register control	05H	00H
RSR	RX register status	06H	00H
ROCR	Receive overflow counter register	07H	00H
BPTR	Back pressure threshold register	08H	37H
FCTR	Flow control threshold register	09H	38H
FCR	RX Flow register control	0AH	00H
EPCR	EEPROM & PHY register control	0BH	00H
EPAR	EEPROM & PHY register address	0CH	40H
EPDRL	EEPROM & PHY Low byte data register	0DH	xxH
EPDRH	EEPROM & PHY High byte data register	0EH	xxH
WCR	Wake Up Control Register (in 8-bit mode)	0FH	00H
PAR	Physical Address Register	10H~15H	Determined by eeprom
MAR	Multicast address register	16H-1DH	xxH
GPCR	General Purpose Control Register (in 8-bit mode)	1EH	01H
GPR	General Purpose Register	1FH	xxH
TRPAL	TX SRAM Read Pointer Address Low Byte	22H	00H
TRPAH	TX SRAM Read Pointer Address High Byte	23H	00H
RWPAL	RX SRAM Write Pointer Address Low Byte	24H	00H
RWPAH	RX SRAM Write Pointer Address High Byte	25H	0CH
VID	Vendor ID	28H~29H	0A46H
PID	Product ID	2AH~2BH	9000H
CHIPR	CHIP Revision	2CH	19H

TCR2	TX Control Register 2	2DH	00H
OCR	Operation Control Register	2EH	00H
SMCR	Special Mode Control Register	2FH	00H
ETXCSR	Early Transmit Control/Status Register	30H	00H
TCSCR	Transmit Check Sum Control Register	31H	00H
RCSCSR	Receive Check Sum Control Status Register	32H	00H
MPAR	MII PHY Address Register	33H	00H
LEDCR	LED Pin Control Register	34H	00H
BUSCR	Processor Bus Control Register	38H	61H
INTCR	INT Pin Control Register	39H	00H
SCCR	System Clock Turn ON Control Register	50H	00H
RSCCR	Resume System Clock Control Register	51H	XXH
MRCMDX	Memory data pre-fetch read command without address increment register	F0H	XXH
MRCMDX1	Memory data read command with address increment register	F1H	XXH
MRCMD	Memory data read command with address increment register	F2H	XXH
MRRL	Memory data read address register low byte	F4H	00H
MRRH	Memory data read address register high byte	F5H	00H
MWCMDX	Memory data write command without address increment register	F6H	XXH
MWCMD	Memory data write command with address increment register	F8H	XXH
MWRL	Memory data write address register low byte	FAH	00H
MWRH	Memory data wirte address register high byte	FBH	00H
TXPLL	TX Packet Length Low Byte Register	FCH	XXH
TXPLH	TX Packet Length High Byte Register	FDH	XXH
ISR	Interrupt Status Register	FEH	00H
IMR	Interrupt Mask Register	FFH	00H

PHY Register

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	CONTROL	Reset	Loop back	Speed select	Auto-N Enable	Power Down	Isotate	Restart	Full Duplex	Col. Test	Reservered						
		0	0	1	1	0	0	0	1	0	000_0000						
01	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reservered				Pream. SuPR.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
		0	1	1	1	1	0000				1	0	0	1	0	0	1
02	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
03	PHYID2	1	0	1	1	1	0	Model No.					Version No.				
								01010					0000				
04	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remade Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05	Link Part Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Panter Protocol Selector Field				
06	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next St Mch	Next Pg Able	Next Pg Rcv	LP AutoN Cap.
16	Specificed config.	BP 4858	BP SCR	BP ALIGN	BP_ADP OK	Reserve d	TX	Reserved	Reserved	Force 100LINK	Reserved	Reserved	RPDCTR -EN	Reset St Mch	Pream. Supr.	Sleep mode	Remote LoopOut
17	Specificed Con#Stat	100 FDX	100 HDX	10 FDX	10 HDX	Reserve d	Reserved	Reserved	PHY ADDR[4.0]					Auto-N. Monitor Bit[3.0]			
18	10T Con#Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	Reserved	Reserved									Potaty Reserse
19	PWDOR	Reserved							PD10DRV	PD1001	Pdchip	Pdaim	Pdaeq	PDdrv	Pdedi	Pdedo	PD10
20	Specificed config.	TSTSE 1	TSTSE2	FORCE_T XSD	FORCE_ FEF	Reserved				Mdx_CNTL	AutoNe g_iptik	Mdx_tx value	Mdx_down	MonSet1	MonSet0	Reserved	PD_vatue

Function Description

Host Interface

Host interface is a general processor local bus interface. Chip selection signal CS # is used to select CBM1001. CS # defaults to low effective, and the polarity can be changed through EEPROM setting. The host can multiplex SD signals through two ports, one is index and the other is data. When CMD = 0, SD represents index information; When CMD = 1, SD indicates data information. Index is the address information of the register to be accessed. You need to set index information before accessing any register.

DMA Control

Cbm1001 provides DMA support to simplify access to internal Register. After configuring the starting address of the Register, first send a dummyread / write command to load the current data into the internal data buffer, and then access the target address through the read / write command. The address will be automatically incremented in 8-bit or 16 bit mode. The data of the next address is automatically loaded into the data buffer.

The internal memory size is 16K bytes. The first 3K bytes are used for sending and the last 13KB bytes are used for receiving.

Packet Transmission

Txsram can store two packages,named index I and index II respectively. Index register02h controls the insertion of CRC and pads. The status is recorded in the 03h and 04H registers. After hardware or software reset, the sending start address is 00h, and index I is valid.

First write data to TX SRAM, and then write data size to byte_ Count register fch and fdh. After setting Bit1 of control register, CBM1001 starts sending index I packet. Before the index I packet is sent, the packet data of index II can be written to TX SRAM. After the index I packet is sent, the byte of index II can be set immediately_ Bit1 of count and control register. In this way, index I and index II can be sent alternately.

Packet Reception

RX SRAM is a ring structure. After hardware or software reset, the starting address of Rx SRAM is at C00h. Each package has 4-byte header, followed by received data, including CRC data. The header structure is 01h, status, byte_ count low, byte_ count high。

Transceiver Operation

- 100BaseTX Operation

Sending includes 4b5b encoder, scrambler, parallel to serial converter, NRZ to NRZI conversion, NRZI to MLT-3 conversion, and finally driving signal to cable through MLT-3 driver.

The receiver includes signal decodeck, digital adaptive equalizer, MLT-3 to binary decoder, clock recovery module, NRZI to NRZ decoder, serial to parallel converter, descrambler descrambling, coding alignment and 4B5b decoder.

- 10Base-T Operation

10Base-T transceiver conforms to IEEE802.3u standard. When CBM1001 works in 10Base-T mode, the coding scheme is Manchester coding.

Electrical Characteristics

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Conditions
D_{VDD}	Supply Voltage	3.135	3.465	V	
T_A	Ambient Temperature	0	70	℃	
P_D (Power Dissipation)	100BASE-TX	-	87	mA	3.3V
	10BASE-T TX(100% utilization)	-	92	mA	3.3V
	10BASE-T idle	-	38	mA	3.3V
	Auto-negotiation	-	56	mA	3.3V
	Power Reduced Mode(without cable)	-	31	mA	3.3V
	Power Down Mode	-	21	mA	3.3V
	Power Down Mode (system clock off)	-	7	mA	3.3V

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Inputs						
V_{IL}	Input Low Voltage	-	-	0.8	V	
V_{IL}	Input High Voltage	2.0	-	-	V	
I_{IL}	Input Low Leakage Current	-1	-	-	uA	V_{IN}=0.0V
I_{IH}	Input High Leakage Current	-	-	1	uA	V_{IN}=3.3V
C_{IN}	Enter the capacity	4	5	6	pf	
Outputs						
V_{OL}	Output Low Voltage	-	-	0.4	V	I_{OL}=4mA
V_{OH}	Output High Voltage	2.4	-	-	V	I_{OH}=-4mA
Receiver						
V_{ICM}	RX+/RX-Common Mode Input Voltage	-	2.5	-	V	100Ω Termination Across
Transmitter						
V_{TD100}	100TX+/-Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
V_{TD10}	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
I_{TD100}	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	Absolute Value

AC Characteristics

- TP Interface

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$T_{TR/F}$	100TX+/- Differential Rise/Fall Time	3.0	-	5.0	ns	
T_{TM}	100TX+/-Differential Rise/Fall Time Mismatch	0	-	0.5	ns	
T_{TDC}	100TX+/- Differential Output Duty Cycle Distortion	0	-	0.5	ns	
$T_{t/T}$	100TX+/-Differential Output Peak-to-Peak Jitter	0	-	1.4	ns	
X_{OST}	100TX+/-Differential Voltage Overshoot	0	-	5	%	

- Crystal Timing

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
T_{CKC}	OSC Clock Cycle	39.998	40	40.002	ns	50ppm
T_{PWH}	OSC Pulse Width High	16	20	24	ns	
T_{PWL}	OSC Pulse Width Low	16	20	24	ns	

- **Processor Read Timing**

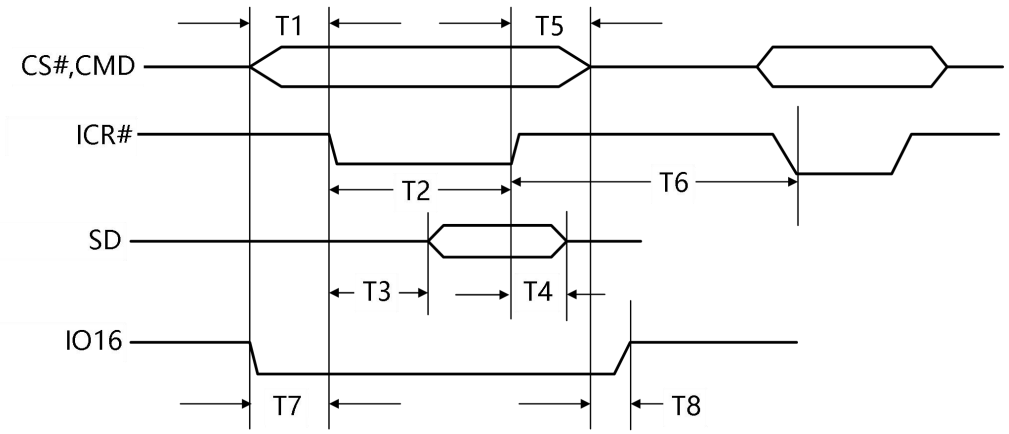

Figure 4. Processor Read Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_1	CS#,CMD valid to IOR# valid	0			ns
T_2	IOR# width	10			ns
T_3	System Date(SD) Delay time			3	ns
T_4	IOR# invalid to System Date(SD) invalid			3	ns
T_5	IOR# invalid to CS#,CMD invalid	0			ns
T_6	IOR# invalid to next IOR#/IOW# valid When read CBM1001	2			clk*

	register				
T_6	IOR# invalid to next IOR#/IOW# valid When read CBM1001 memory withF2h register	4			clk*
T_2+T_6	IOR# invalid to next IOR#/IOW# valid When read CBM1001 memory with F2h register	1			clk*
T_7	CS#,CMD valid to IO 16 valid			3	ns
T_8	CS#,CMD invalid to IO16 invalid			3	ns

- **Processor Write Timing**

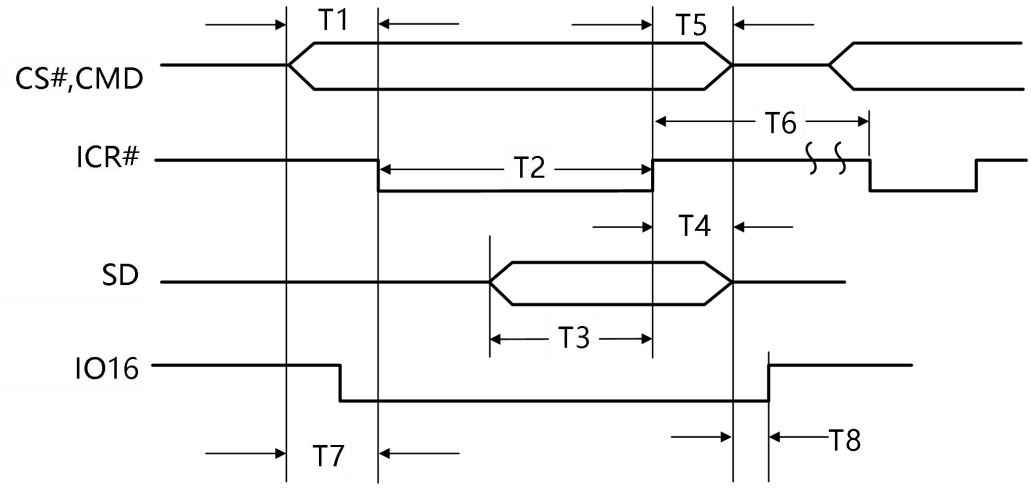

Figure 5. Processor Write Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_1	CS#,CMD valid to IOW# valid	0			ns
T_2	IOW# width	10			ns
T_3	System Date(SD) Setup time	10			ns
T_4	System Date(SD) Hold time	3			ns
T_5	IOW # Invalid to CS#,CMD invalid	0			ns
T_6	IOW# invalid to next IOW#/IOR# valid When write CBM1001 INDEX port	1			clk*
T_6	IOW# Invalid to next IOW#/IOR# Valid When write CBM1001 memory DATE port	2			clk*
T_2+T_6	IOW# Invalid to next IOR#/IOW# valid When write CBM1001 memory	1			clk*
T_7	CS#,CMD valid to IO 16 valid			3	ns
T_8	CS#,CMD invalid to IO16 invalid			3	ns

- EEPROM Interface Timing

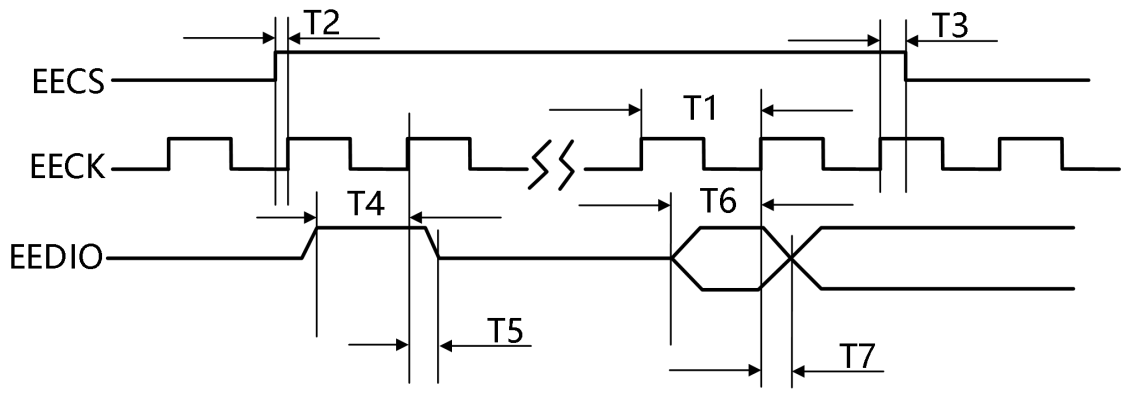

Figure 6. EEPROM Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_1	EECK Frequency		0.375		Mhz
T_2	EECS Setup Time		500		ns
T_3	EECS Hold Time		2166		ns
T_4	EEDIO Setup Time when output		480		ns
T_5	EEDIO Hold Time when output		2200		ns
T_6	EEDIO Setup Time when input	8			ns
T_7	EEDIO Hold Time when input	8			ns

Applications Information

Auto MDIX Notes

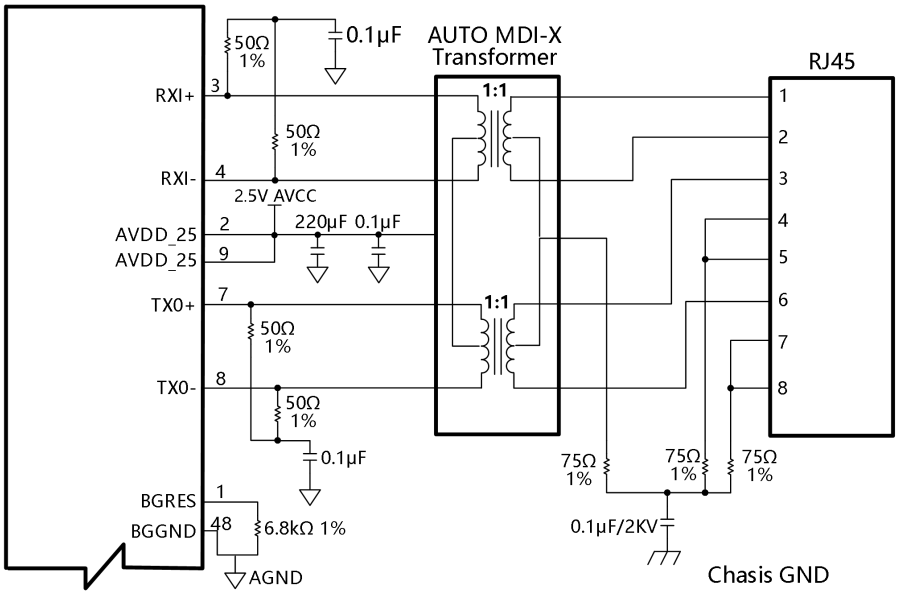

Figure 7. Auto MIDX Notes

Non auto MDIX Notes

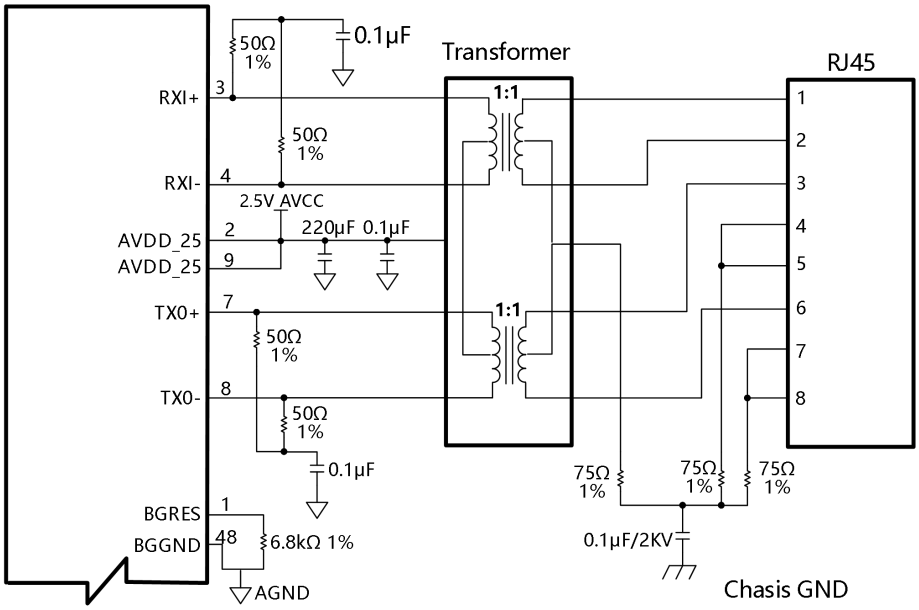

Figure 8. Non Auto MIDX Notes

Package Outline Dimensions

TQFP-48

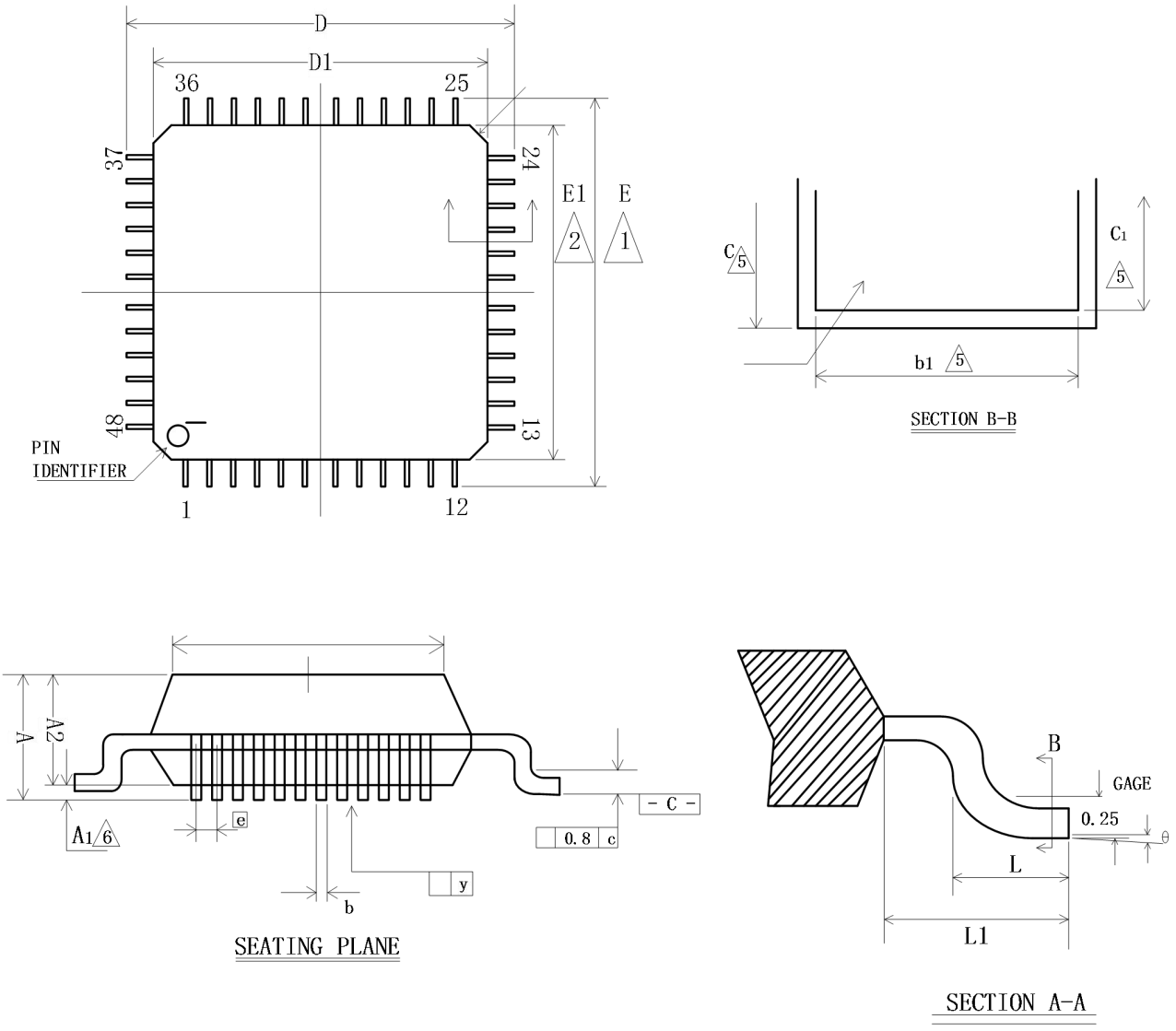

Figure 9. 48-Lead Outline Package [TQFP]

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.063	-	-	1.60
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
b1	0.007	0.008	0.009	0.17	0.20	0.23
C	0.004	-	0.008	0.09	-	0.20
C1	0.004	-	0.006	0.09	-	0.16
D	0.354 BSC			9.00 BSC		
D1	0.276 BSC			7.00 BSC		
E	0.354 BSC			9.00 BSC		
E1	0.276 BSC			7.00BSC		
e	0.020 BSC			0.50 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039 REF			1.00 REF		
y	0.003 MAX			0.08 MAX		

1. To be determined at seating plane.
2. Dimensions D1 and E1 do not include mold protrusion.D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimensions b does not include dambar protrusion. Total in excess of the b dimensions at maximum material condition. Dambar cannot be located on the lower radius of the foot.
4. Exact shape of each corner is optional.
5. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
6. A1 is defined as the distance from the seating plane to the lowest point of the package body.
7. Controlling dimension: millimeter.
8. Reference documents：JEDECMS-026，BBC。

Package/Ordering Information

PRODUCT TYPE	OPERATING TEMPERTURE	PACKAGE	PAKEAGE MARKING	NUMBER OF PACKAGES
CBM1001A-Q	0℃~70℃	TQFP-48	CBM1001A-Q	Tray, 1000